What is claimed is:

1. An input buffer circuit of a synchronous semiconductor memory device comprising a differential amplifier type input buffer and a low current type input buffer, wherein the differential amplifier type input buffer is operated in a normal mode, and the low current type input buffer is operated in a self-refresh mode, thereby rducing the current flowing through the input buffer in the self-refresh mode

2. An input buffer of a synchronous semiconductor memory device, comprising:

a first input buffer circuit that receives an external clock enable signal and a self-refresh control signal to amplify a voltage difference between the received external clock enable signal and a first reference voltage;

a delay circuit that receives the self-refresh control signal to output a delayed self-refresh control signal;

a second input buffer that receives the external clock enable signal and the delayed self-refresh control signal to amplify a voltage difference between the received external clock enable signal and a second reference voltage; and

an OR circuit that receives the output signal of the first input buffer and the output signal of the second input buffer and then performs an OR operation to output an internal clock enable signal, wherein the first input buffer is operated in the normal mode and the second input buffer is operated in the self-refresh mode to thereby reduce the current flowing into the input buffer in the self-refresh mode, and wherein the first input buffer is a differential amplifier type input buffer and the second input buffer is a low current type input buffer.

3. The input buffer circuit according to claim 2, wherein the second input buffer is a Bazes type input buffer.

4. The input buffer circuit according to claim 2, wherein the first input buffer comprises:

a first differential amplifier that receives the external clock enable signal and the first reference voltage and generates an output signal based on a voltage difference between the external clock enable signal and the first reference voltage;

a first inverter for inverting the self-refresh control signal;

a first NMOS transistor having a gate terminal that receives the output signal of the first inverter, a drain terminal connected to the first differential amplifier and a source terminal connected to a ground voltage; and

a first PMOS transistor having a gate terminal that receives the output signal of the first inverter, a source terminal connected to a power supply voltage and a drain terminal connected to an output terminal of the first differential amplifier.

5. The input buffer circuit according to claim 2, wherein the first input buffer comprises:

a first differential amplifier that receives the external clock enable signal and the first reference voltage and generates an output signal based on a voltage difference between the external clock enable signal and the first reference voltage;

a first PMOS transistor having a gate terminal that receives the external clock signal, a drain terminal connected to the first differential amplifier and a source terminal

connected to the power supply voltage; and.

a first NMOS transistor having a gate terminal that receives the external clock enable signal, a source terminal connected to the ground voltage and a drain terminal connected to the output terminal of the first differential amplifier.

6. The input buffer circuit according to claim 2, wherein the second input buffer comprises:

a first differential amplifier that receives the external clock enable signal and the second reference voltage and generates an output signal based on a voltage difference between the external clock enable signal and the second reference voltage;

a first inverter for inverting the delayed self-refresh control signal;

a first PMOS transistor having a gate terminal that receives the output signal from the first inverter, a drain terminal connected to the first differential amplifier and a source terminal connected to a power supply voltage; and

a first NMOS transistor having a gate terminal that receives the output signal from the first inverter, a source terminal connected to the ground voltage and a drain terminal connected to an output terminal of the first differential amplifier.

7. The input buffer circuit according to claim 6, wherein the first differential amplifier, comprises:

a second PMOS transistor having a source terminal connected to the drain terminal of the first PMOS transistor and a gate terminal connected to a first node;

a third PMOS transistor having a source terminal connected to the drain terminal of the second PMOS transistor, a gate terminal to which the external clock enable signal is supplied, and a drain terminal connected to the first node;

a fourth PMOS transistor having a source terminal connected to the drain terminal of the second PMOS transistor and a gate terminal to which the second reference voltage is supplied;

a second NMOS transistor having a drain terminal connected to the first node and a gate terminal to which the external clock enable signal is supplied;

a third NMOS transistor having a drain terminal connected to the drain terminal of the fourth PMOS transistor and a gate terminal to which the second reference voltage is supplied; and

a fourth NMOS transistor having a drain terminal commonly connected to the source terminals of the second NMOS transistor and the third NMOS transistor, a gate terminal connected to the first node and a source terminal to which the ground voltage is supplied, wherein an output signal of the first differential amplifier is output from the drain terminal of the third PMOS transistor.